Homework 6

<Counter Design>

Using only one 3-bit binary counter with clear input and minimum number of components listed in below, design a counter that generates the following sequence repeatedly:

0->2 -> 4 -> 6 -> 8 -> 10 -> 12 -> 0 -> 2 -> 4 ……

Note:

E is enable input. When E = 1, it counts at every clock cycle. When E = 0, it stops counting and output stays unchanged.

clr is clear input. When clr = 1, it starts counting from 0 from the next clock cycle if E = 1.

The allowed components are

a) 3-bit binary counter

b) Shifter (left shifter, right shifter)

c) Logic Gates (And, Or, Not)

Note: the number of input pins is not limited which means that you can have more than 2 input pins. If you want to use shifter, you can use the shifter representation

shown as follows.

